**Prelab:**

Design a voltage divider biased CE stage with emitter degeneration. That stage should support a voltage gain of 5 and an input impedance larger than 3 KOhms with a bias current of 0.5 mA. Assume Beta=100, Is = 5e-17. Neglect the early voltage effect. You also need to provide values for the operating point of this transistor. Find the output resistance of this stage if the early voltage = 20 V.

**Part#1: LTspice BJT netlist commands:**

LTspice offers the ability to use BJT transistors in a circuit through net-listing. The following is how you add a BJT transistor to your netlist:

1. The syntax **(Q1 C1 B1 E1 my-npn)** Assigns nodes C1 (collector node for Q1 transistor), B1 (Base node for Q1 transistor) and E1 (Emitter node for Q1 transistor). “my-npn” is the name of the transistor that will be used to specify the transistor parameters such as Is, VA, Beta etc. For a complete list of the BJT parameters and their specific symbols visit this webpage” <https://www.youspice.com/spice-modeling-of-a-bjt-from-datasheet/>”.
2. The above syntax line in step “a” should be followed by this line “**.model my-npn npn (BF= xx, IS = xx, VJC = xx)”**. This syntax creates a transistor model called my-npn and allows you to enter its specific parameters.
3. After the model is created you should be able to use the transistor nodes (E1,B1,C1) to connect with the rest of the elements in your circuit. i.e. this netlist shows a resistive divider biased npn transistor with a sinusoidal input voltage coupled to the transistor through Cin capacitor.

(Q1 C1 B1 E1 my-npn)

.model my-npn npn (BF= xx, IS = xx, VJC = xx)

Vin Vin 0 SIN(x x x)

Vcc 4 0 x

Rc 4 C1 x

Re E1 0 x

R1 4 B1 x

R2 B1 0 x

Cin Vin B1 x

**Part #2: CE stage testing**

1. Use the skills that you have learned from the previous part to model the CE stage in the pre-lab.
2. Perform a DC analysis assuming Vcc = 2.5 V. Check the differences between your calculated values and the simulated values and justify the difference. Make sure that no AC sources are added to your simulation when performing your DC analysis.
3. Add an AC source without a coupling capacitor to your netlist and perform a transient analysis. The source peak voltage is 1mV with a 500 Hz frequency and a 0 DC offset. Also attach the output to a load resistance of 100 MOhms without using a coupling capacitor.
4. Perform a Transient analysis from 0 - 0.01 seconds with a step size of 0.1 msec.
5. Using ADD traces compare the input voltage to the output voltage and observe the amplification. Justify your observation.
6. Repeat “c, d” but this time add input/output coupling capacitors. (The coupling capacitors should be in the micro-farad range i.e 1 micro-farad). Justify the observed amplification using the voltage gain equation for a CE stage.
7. Also, observe the phase difference between the input and output voltages.
8. Change the input frequency to 10 Hz and observe the effects on the amplification and the phase shift. Justify your observations. Repeat this process for a 1 MHz frequency.
9. Increase the AC input level to 1 V and fix the frequency at 500 Hz. What did you notice? Why?
10. Fix the AC input level at 1 mV and 500 Hz and change the DC offset to -1 V/ +1V. Justify your observations.
11. With an AC input of 1 mV, 500 Hz and 0 DC offset, add a bypass capacitor to the CE stage. Choose a capacitor of 1 micor-farad and observe what happens to the gain. change the value of the capacitor to 1 mF and record any significant differences.
12. Change the load resistance from 100MOhms to 10 Ohms and observe the difference and justify it.

**Part #3: Measuring the input and output resistances:**

LTspice netlist can be used to measure any quantities and perform math operations at any part of your circuit using the commands “.meas” and “PARAM”.

For instance, if we want to measure the input resistance of an amplifier, we need to find Rin = vx/ix, where vx is a small change applied to the input and ix is the corresponding input current. We also have to ensure that the amplifier is not loaded. This can be done using our previous netlist in part #2 by detaching the load and the output coupling capacitor while keeping the AC input source attached to the circuit. The AC source will be responsible for generating vx = Vin, and ix = Iin (the input current), the following allows you to measure the input resistance:

.meas vmax MAX V(Vin)

.meas imax MAX I(Vin)

.meas r\_in PARAM = 'vmax/imax'

The “PARAM” function allows you to perform mathematical operations within the netlist environment.

1. Using the above explanation, find Rin for the CE stage with emitter degeneration. Show that the simulation results are very similar to the calculated results. (You can view the simulation results by accessing Spice error log)
2. Repeat the above to find Rin without emitter degeneration by adding the bypass capacitor.
3. Find Rout neglecting the early voltage. This should be done by shorting the input and adding a variable source to the output via a coupling capacitor.
4. Find Rout if the early voltage = 20 V. The early voltage effect is added to the netlist by adding VAF = 20 to the transistor parameters.

**Deliverables:**

1. All plots, netlist and error logs that display your simulation results for every part in this experiment.
2. All necessary justifications for every part in this experiment. Your justifications should also use mathematical arguments that relate theory to simulation.